PATENT

Case Docket No. ASMMC.047AUS
Date: February 20, 2004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Hannu Huotari
Appl. No.	:	10/601,037
Filed	:	June 19, 2003
For	:	METHOD TO FABRICATE DUAL METAL CMOS DEVICES
Examiner	:	Unknown
Group Art Unit	:	2811

I hereby certify that this correspondence and all marked attachments are being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on

February 20, 2004
(Date)

Andrew N. Merickel, Reg. No. 53,317

TRANSMITTAL LETTER

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-identified application are the following documents:

(X) An Information Disclosure Statement;
(X) A PTO Form 1449 listing thirteen (13) references, copies of which are enclosed; and
(X) A return prepaid postcard.

The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment, to Account No. 11-1410.

Andrew N. Merickel
Registration No. 53,317
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(415) 954-4114

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INFORMATION DISCLOSURE STATEMENT

Applicant	:	Hannu Huotari
App. No.	:	10/601,037
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Examiner	:	Unknown
Group Art Unit	:	2811

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed is form PTO-1449 listing thirteen (13) references that are also enclosed.

This Information Disclosure Statement is being filed before the receipt of a first Office Action on the merits, and presumably no fee is required in accordance with 37 C.F.R. § 1.97(b)(3). If a first Office Action on the merits was mailed before the mailing date of this Statement, the Commissioner is authorized to charge the fee set forth in 37 C.F.R. § 1.17(p) to Deposit Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: February 20, 2004

By: _____

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(415) 954-4114

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FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT (USE SEVERAL SHEETS IF NECESSARY)	ATTY. DOCKET NO. ASMMC.047AUS	APPLICATION NO. 10/601,037
	APPLICANT Hannu Huotari	
	FILING DATE June 19, 2003	GROUP ART UNIT 2811

EXAMINER INITIAL		OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)
	1.	Chatterjee et al., "CMOS Metal Replacement Gate Transistors using Tantalum Pentoxide Gate Insulator," IEEE, IEDM, 0-7803-4774-9/98, pp. 777-780 (1998)
	2.	Chen et al., "0.18μm Metal Gate Fully-Depleted SOI MOSFETs for Advanced CMOS Applications," Symposium on VLSI Technology Digest of Technical Papers, pp. 25-26 (1999)
	3.	Ducroquet et al., "Full CMP Integration of CVD TiN Damascene Sub-0.1-μm Metal Gate Devices For ULSI Applications," IEEE Transactions on Eectron Devices, Vol 48, No. 8, pp. 1816-1821 (2001)
	4.	Ferguson et al., "Titanium Nitride Metal Gate Electrode: Effect of Nitrogen Incorporation," Advanced Metallization Conference 2001 (AMC 2001), pp. 115-119
	5.	Hobbs et al., "Sub-Quarter Micron CMOS Process for TiN-Gate MOSFETs with TiO2 Gate Dielectric formed by Titanium Oxidation," Advanced Products Research and Development Lab, Symposium on VLSi Technology Digest of Technical Papers, pp. 133-134 (1999)
	6.	Maiti et al., "PVD TiN Metal Gate MOSFETs on Bulk Silicon and Fully Depleted Silicon-On-Insulator (FDSOI) Substrates for Deep Sub-Quarter Micron CMOS Technology," IEEE, IEDM, 0-7803-4774-9/98, pp. 781-784 (1998)
	7.	Park et al., "Robust Ternary Metal Gate Electrodes for Dual Gate CMOS Devices," IEEE, IEDM, 0-7803-7050-3/02, pp. 671-674 (2001)
	8.	Polishchuk, "Dual Work Function Metal Gate CMOS Technology Using Metal Interdiffusion," IEEE Electron Device Letter, Vol. 22, No. 9 pp, 444-446 (2001)
	9.	Wakabayashi et al., "A Novel W/TiNx Metal Gate CMOS Technology using Nitrogren-Concentration-Controlling TiNx Film," IEEE, IEDM, 0-7803-5410-9/99, pp. 253-256 (1999)
	10.	Yagishita et al., "High Performance Damascene Metal Gate MOSFET's for 0.1 μm Regime," IEEE Transactions on Electron Devices, Vol. 47, No. 5, pp. 1028-1034 (2000)
	11.	Yagishita et al., "Reduction of Threshold Voltage Deviation in Damascene Metal Gate MOSFETs," IEEE, IEDM, 0-7083-5410-9/99, pp. 257-260 (1999)
	12.	Yeo et al., "Dual-Metal Gate CMOS Technology with Ultrathin Silicon Nitride Gate Dielectric," IEEE Electronic Device Letters, Vol. 22, No. 5, pp. 227-229 (2001)
	13.	Zhong et al., "Electrical Properties of RuO_2 Gate Electrodes for Dual Metal Gate Si-CMOS," IEEE Electron Device Letters, Vol. 21, No. 12, December 2000, pp. 593-595

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EXAMINER	DATE CONSIDERED

*EXAMINER: INITIAL IF CITATION CONSIDERED, WHETHER OR NOT CITATION IS IN CONFORMANCE WITH MPEP 609; DRAW LINE THROUGH CITATION IF NOT IN CONFORMANCE AND NOT CONSIDERED, INCLUDE COPY OF THIS FORM WITH NEXT COMMUNICATION TO APPLICANT.